

WHAT IS CLAIMED IS:

1 1. A voltage controlled oscillator (VCO) comprising a ring oscillator having an
2 input, an output, an odd number M of complementary metal oxide semiconductor
3 (CMOS) inverters series coupled between the input and output, a feedback connection
4 between the input and output, and a number K of voltage controlled feedforward (FF)
5 stages, each of the K FF stages coupled in parallel with K groups of an odd number of
6 G sequential CMOS inverters selected from the M CMOS inverters, each of the K FF
7 stages having a plurality P channel metal oxide silicon transistors (PFETs) and a
8 plurality of N channel metal oxide silicon transistors (NFETs), at least one of the
9 PFETs having a first isolated region of semiconductor material (body) connected to a
10 first body terminal, and at least one of the NFETs having a second isolated body
11 connected to a second body terminal, wherein the K FF stages are controlled by first
12 and second control voltages coupled to the first and second body terminals
13 respectively.

1 2. The VCO of claim 1, wherein each of the K FF stages comprises a CMOS
2 inverter stage coupled in series with a transfer gate stage having a parallel connection
3 of a first PFET and a first NFET.

1 3. The VCO of claim 2, wherein the first PFET of the transfer gate stage has a
2 body terminal coupled to the first control voltage and the NFET of the transfer gate a
3 body terminal coupled to the second control voltage.

1 4. The VCO of claim 1, wherein the second control voltage is derived from the
2 first control voltage such that the first and the second control voltages have a same
3 nominal value and opposite slopes when modified.

1 5. The VCO of claim 2, wherein each of the CMOS inverters in the K FF stages
2 comprise a second PFET and a second NFET coupled in series, wherein the second
3 PFET of at least one of the CMOS inverters has a body terminal coupled to the first
4 control voltage and the second NFET of the at least one of the CMOS inverters has a
5 body terminal coupled to the second control voltage.

1 6. The VCO of claim 3, wherein each of M CMOS inverters comprise a third
2 PFET and a third NFET, wherein the third PFET of at least one of the M CMOS
3 inverters has a body terminal coupled to the first control voltage and the third NFET
4 of the at least one of the M CMOS inverters has a body terminal coupled to the
5 second control voltage.

1 7. The VCO of claim 5, wherein each of M CMOS inverters comprise a third
2 PFET and a third NFET, wherein the third PFET of at least one of the M CMOS
3 inverters has a body terminal coupled to the first control voltage and the third NFET
4 of the at least one of the M CMOS inverters has a body terminal coupled to the
5 second control voltage.

1 8. The VCO of claim 2 wherein each of the CMOS inverters in the K FF stages
2 comprise a second PFET and a second NFET coupled in series, wherein the second
3 PFET of at least one of the CMOS inverters has a body terminal coupled to the first
4 control voltage by a first clamping circuit preventing a body diode coupled to the
5 body terminal of the second PFET from being forward biased and the second NFET
6 of the at least one of the CMOS inverters has a body terminal coupled to the second
7 control voltage by a second clamping circuit preventing a body diode coupled to the
8 body terminal of the second NFET from being forward biased.

1 9. The VCO of claim 3, wherein each of M CMOS inverters comprise a second
2 PFET and a second NFET coupled in series, wherein the second PFET of at least one
3 of the CMOS inverters has a body terminal coupled to the first control voltage by a
4 first clamping circuit preventing a body diode coupled to the body terminal of the
5 second PFET from being forward biased and the second NFET of the at least one of
6 the CMOS inverters has a body terminal coupled to the second control voltage by a
7 second clamping circuit preventing a body diode coupled to the body terminal of the
8 second NFET from being forward biased.

1 10. The VCO of claim 8, wherein the first clamping circuit comprises a clamping
2 PFET having a body terminal coupled to the source of the second PFET, a gate
3 coupled to ground potential, a drain coupled to the body terminal of the second PFET
4 and a source coupled to the first control voltage and the second clamping circuit
5 comprises a clamping NFET having a body terminal coupled to the source of the
6 second NFET, a gate coupled to the positive power supply voltage, a drain coupled to
7 the body terminal of the second NFET and a source coupled to the first control
8 voltage.

1 11. The VCO of claim 9, wherein the first clamping circuit comprises a clamping
2 PFET having a body terminal coupled to the source of the second PFET, a gate
3 coupled to ground potential, a drain coupled to the body terminal of the second PFET
4 and a source coupled to the first control voltage and the second clamping circuit
5 comprises a clamping NFET having a body terminal coupled to the source of the
6 second NFET, a gate coupled to the positive power supply voltage, a drain coupled to
7 the body terminal of the second NFET and a source coupled to the first control
8 voltage.

1 12. The VCO of claim 1, wherein K is equal to M.

1 13. A phase locked loop (PLL) circuit for generating an output clock signal with a
2 frequency that is a multiple number N times the frequency of a reference clock signal,
3 comprising:

4 a voltage controlled oscillator (VCO) generating the output clock signal with a
5 frequency modified in response to a control voltage;

6 a frequency divider for frequency dividing the output clock signal by N,
7 generating a frequency divided clock signal;

8 a phase frequency detector for comparing the frequency divided clock signal
9 to the reference clock signal and generating a phase/frequency error signal; and

10 circuitry for converting the phase/frequency error signal to the control voltage,
11 wherein the VCO is a ring oscillator having an input, an output, an odd number M of
12 complementary metal oxide semiconductor (CMOS) inverters series coupled between
13 the input and output, a feedback connection between the input and output, and a
14 number K of voltage controlled feedforward (FF) stages, each of the K FF stages
15 coupled in parallel with K groups of an odd number of G sequential CMOS inverters
16 selected from the M CMOS inverters, each of the K FF stages having a plurality P
17 channel metal oxide silicon transistors (PFETs) and a plurality of N channel metal
18 oxide silicon transistors (NFETs), at least one of the PFETs having a first isolated
19 region of semiconductor material (body) connected to a first body terminal, and at
20 least one of the NFETs having a second isolated body connected to a second body
21 terminal, wherein the K FF stages are controlled by first and second control voltages
22 coupled to the first and second body terminals respectively.

1 14. The PLL circuit of claim 13, wherein each of the K FF stages comprise a
2 CMOS inverter stage coupled in series with a transfer gate stage having a parallel
3 connection of a first PFET and a first NFET.

1 15. The PLL circuit of claim 14, wherein the first PFET of the transfer gate stage
2 has a body terminal coupled to the first control voltage and the NFET of the transfer
3 gate a body terminal coupled to the second control voltage.

1 16. The PLL circuit of claim 13, wherein the second control voltage is derived
2 from the first control voltage such that the first and the second control voltages have a
3 same nominal value and opposite slopes when modified.

1 17. The PLL circuit of claim 14, wherein each of the CMOS inverters in the K FF
2 stages comprise a second PFET and a second NFET coupled in series, wherein the
3 second PFET of at least one of the CMOS inverters has a body terminal coupled to
4 the first control voltage and the second NFET of the at least one of the CMOS
5 inverters has a body terminal coupled to the second control voltage.

1 18. The PLL circuit of claim 15, wherein each of M CMOS inverters comprise a
2 third PFET and a third NFET, wherein the third PFET of at least one of the M CMOS
3 inverters has a body terminal coupled to the first control voltage and the third NFET
4 of the at least one of the M CMOS inverters has a body terminal coupled to the
5 second control voltage.

1 19. The PLL circuit of claim 17, wherein each of M CMOS inverters comprises a
2 third PFET and a third NFET, wherein the third PFET of at least one of the M CMOS
3 inverters has a body terminal coupled to the first control voltage and the third NFET
4 of the at least one of the M CMOS inverters has a body terminal coupled to the
5 second control voltage.

1 20. The PLL circuit of claim 14, wherein each of the CMOS inverters in the K FF
2 stages comprise a second PFET and a second NFET coupled in series, wherein the

3 second PFET of at least one of the CMOS inverters has a body terminal coupled to
4 the first control voltage by a first clamping circuit preventing a body diode coupled to
5 the body terminal of the second PFET from being forward biased and the second
6 NFET of the at least one of the CMOS inverters has a body terminal coupled to the
7 second control voltage by a second clamping circuit preventing a body diode coupled
8 to the body terminal of the second NFET from being forward biased.

1 21. The PLL circuit of claim 15, wherein each of M CMOS inverters comprise a
2 second PFET and a second NFET coupled in series, wherein the second PFET of at
3 least one of the CMOS inverters has a body terminal coupled to the first control
4 voltage by a first clamping circuit preventing a body diode coupled to the body
5 terminal of the second PFET from being forward biased and the second NFET of the
6 at least one of the CMOS inverters has a body terminal coupled to the second control
7 voltage by a second clamping circuit preventing a body diode coupled to the body
8 terminal of the second NFET from being forward biased.

1 22. The PLL circuit of claim 20, wherein the first clamping circuit comprises a
2 clamping PFET having a body terminal coupled to the source of the second PFET, a
3 gate coupled to ground potential, a drain coupled to the body terminal of the second
4 PFET and a source coupled to the first control voltage and the second clamping
5 circuit comprises a clamping NFET having a body terminal coupled to the source of
6 the second NFET, a gate coupled to the positive power supply voltage, a drain
7 coupled to the body terminal of the second NFET and a source coupled to the first
8 control voltage.

1 23. The PLL circuit of claim 21, wherein the first clamping circuit comprises a
2 clamping PFET having a body terminal coupled to the source of the second PFET, a
3 gate coupled to ground potential, a drain coupled to the body terminal of the second
4 PFET and a source coupled to the first control voltage and the second clamping

5 circuit comprises a clamping NFET having a body terminal coupled to the source of
6 the second NFET, a gate coupled to the positive power supply voltage, a drain
7 coupled to the body terminal of the second NFET and a source coupled to the first
8 control voltage.

1 24. The PLL circuit of claim 13, wherein K is equal to M.

1